Title: INTERFACE CONVERTER
Inventor's Name: NAKANO
Application No.: NEW
Docket No.: 108075-00118

Fig.1

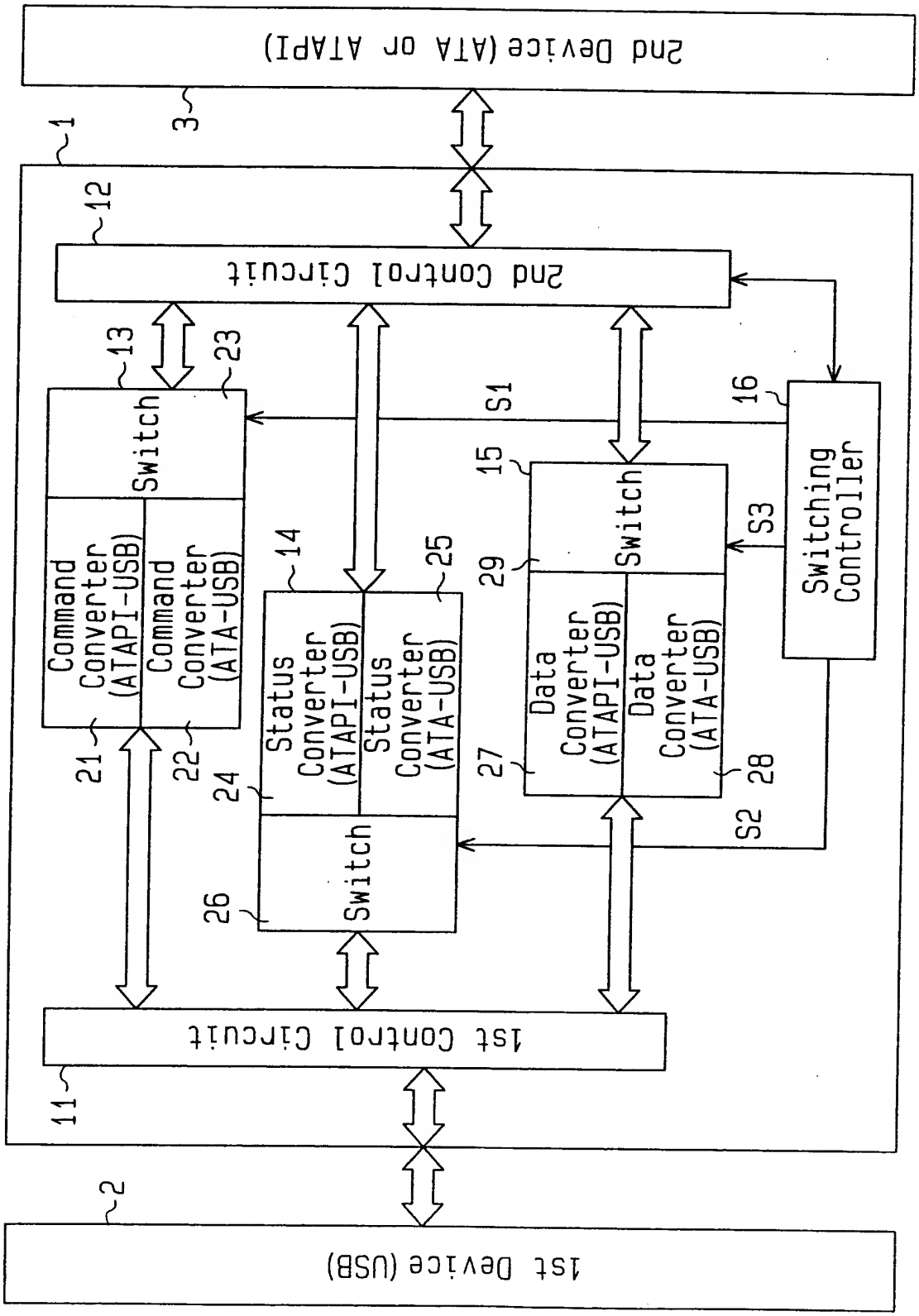

Fig.2

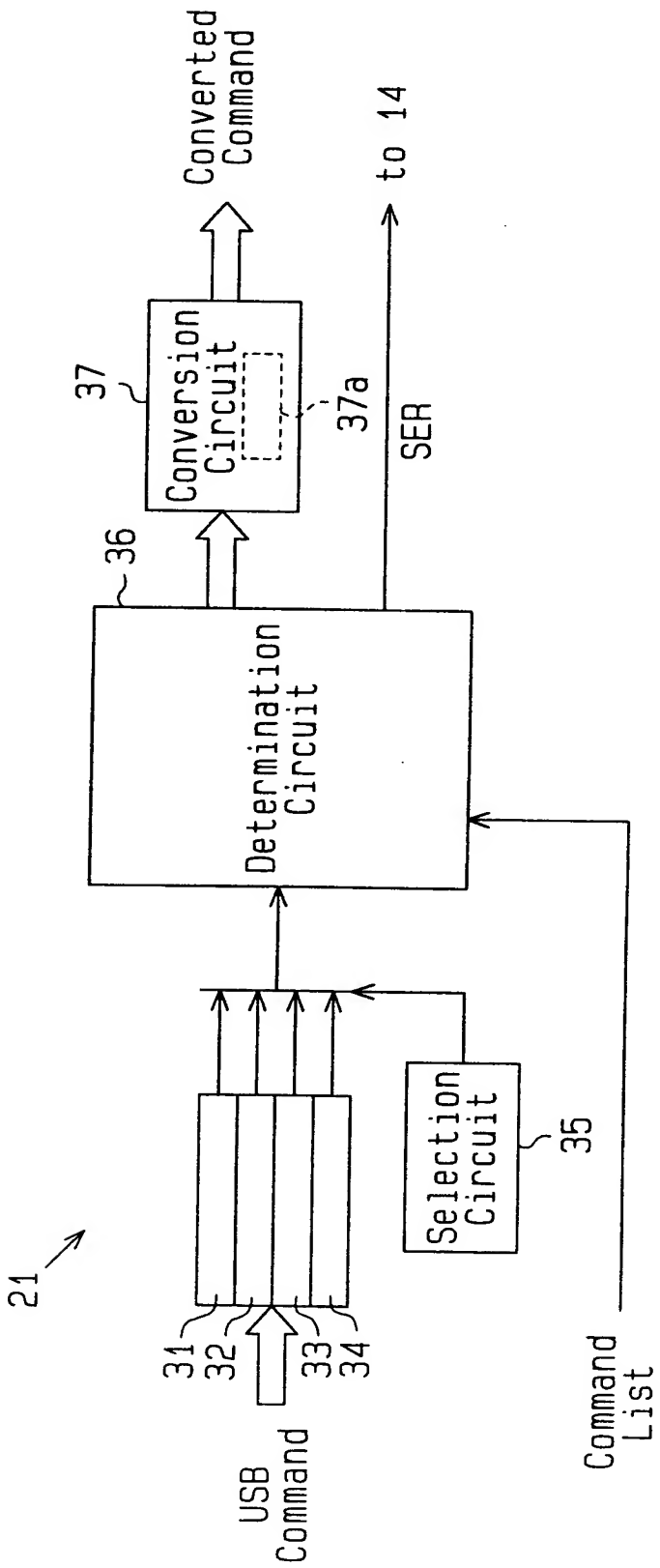
Converted Command
to 14
37
Conversion Circuit
37a
SER
36
Determination Circuit
Selection Circuit
35
21
31
32
33
34
USB Command
Command List

Fig.3

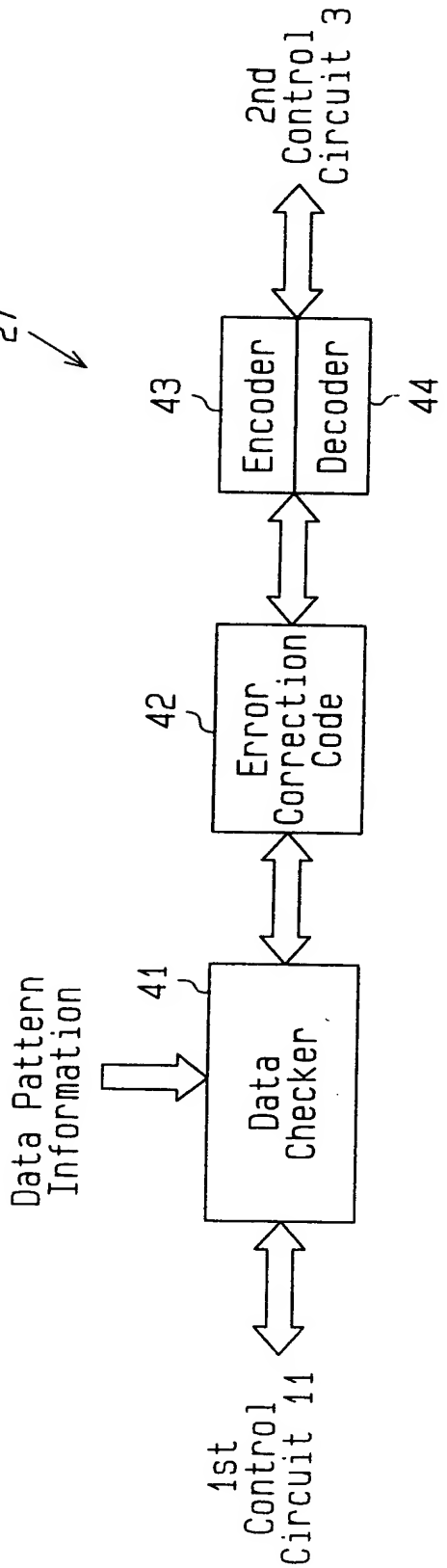
27
2nd Control Circuit 3
43
Encoder
Decoder
44
42
Error Correction Code
41
Data Pattern Information
Data Checker
1st Control Circuit 11

Fig.4

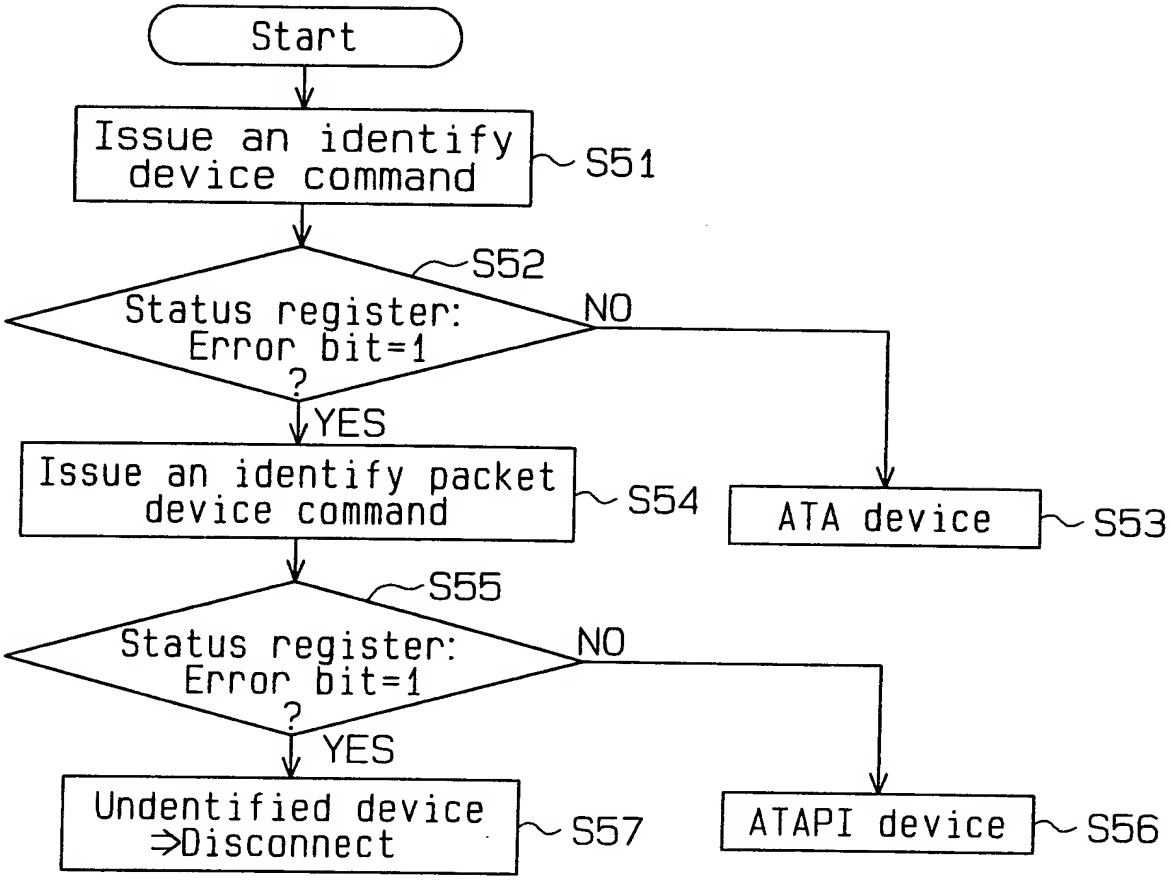
Start
Issue an identify device command
S51
S52
Status register: Error bit=1 ?
NO
YES
Issue an identify packet device command
S54
ATA device
S53
S55
Status register: Error bit=1 ?
NO
YES
Undentified device ⇒Disconnect
S57
ATAPI device
S56

Fig.5

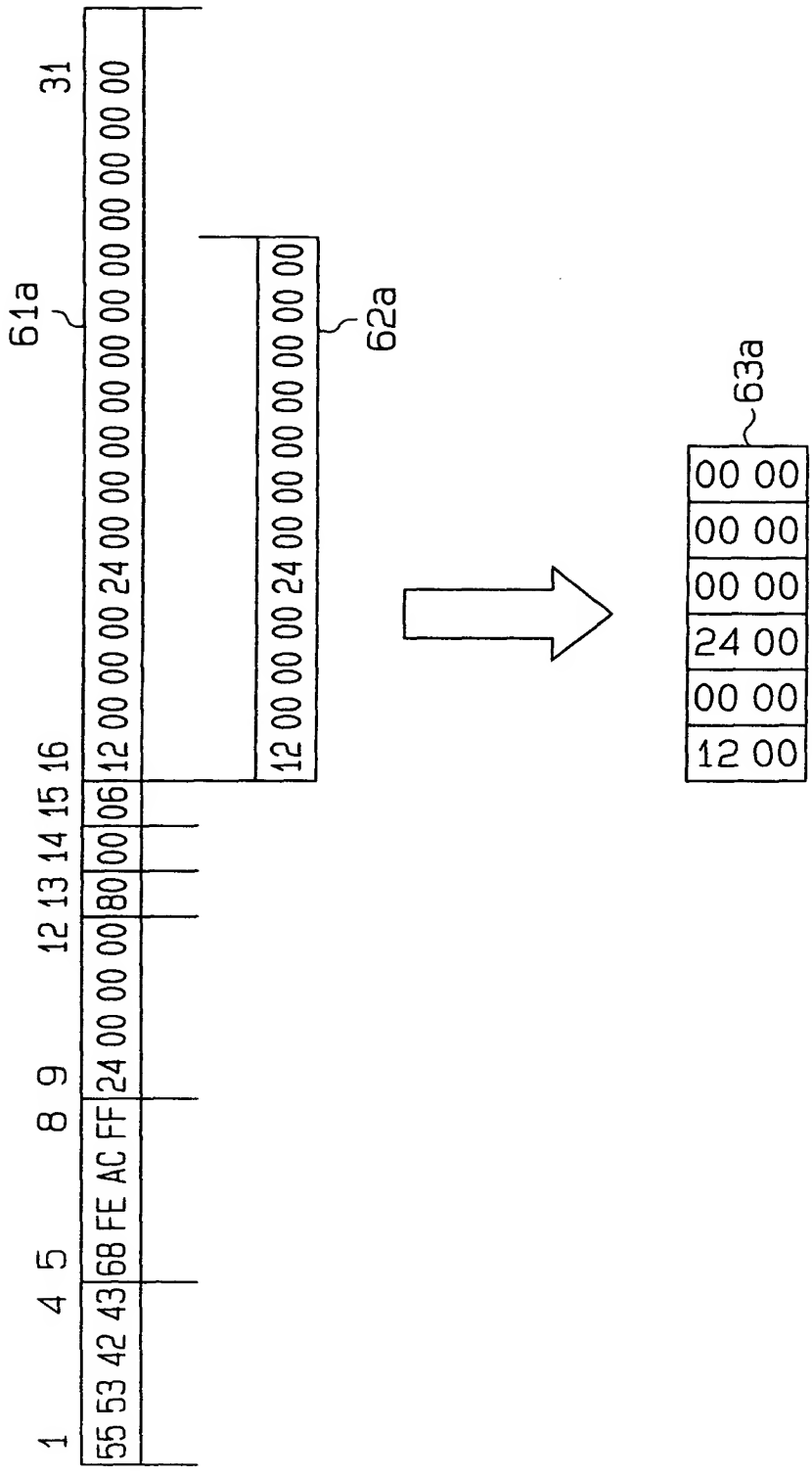
1
4 5
8 9
12 13 14 15 16
31
55 53 42 43 68 FE AC FF 24 00 00 00 80 00 06 12 00 00 00 24 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
61a
12 00 00 00 24 00 00 00 00 00 00 00 00 00 00
62a
63a
00 00
00 00
00 00
24 00
00 00
12 00

Fig.6

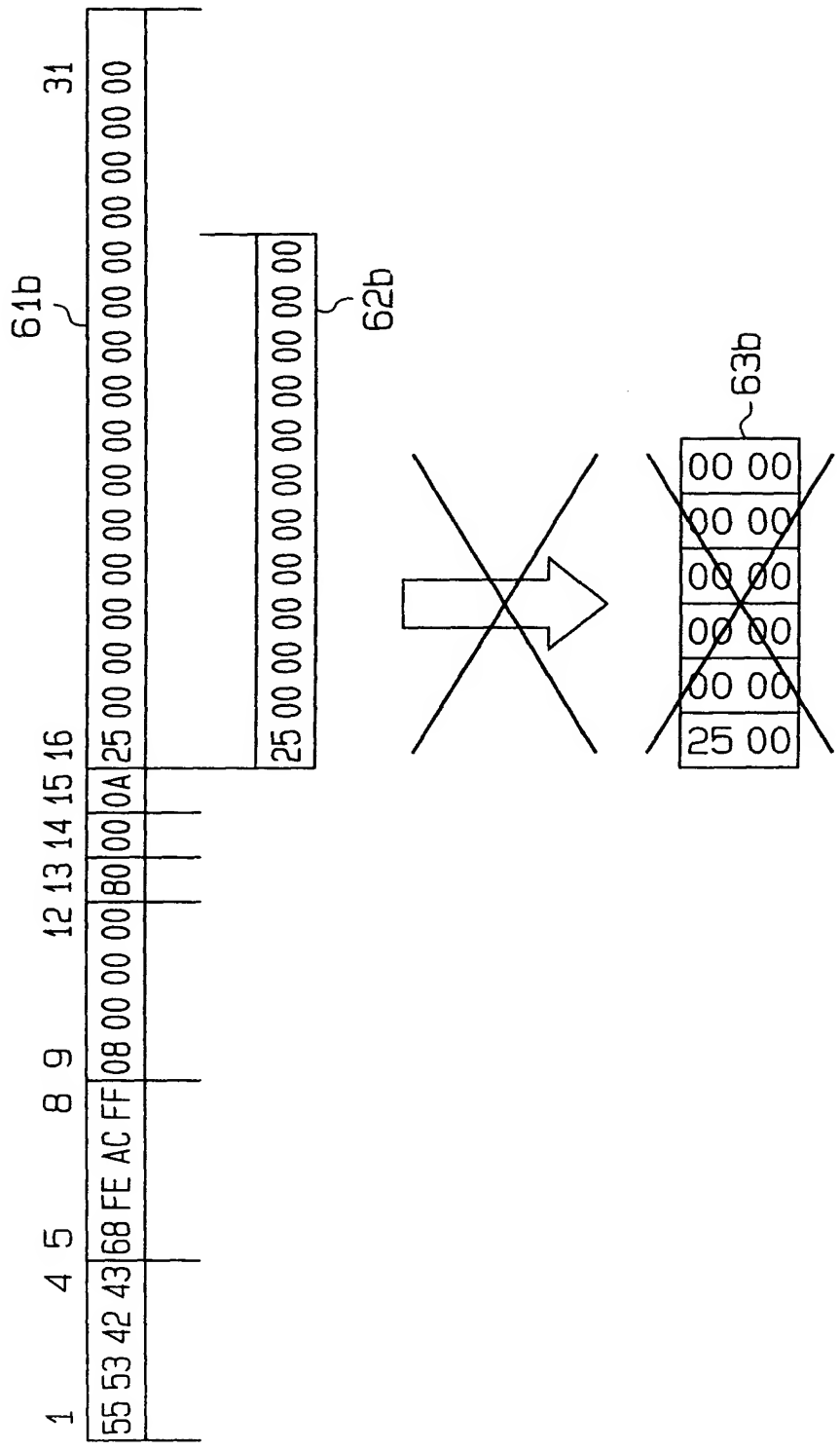
1
4 5
8 9
12 13 14 15 16
31
55 53 42 43 68 FE AC FF 08 00 00 00 80 00 0A 25 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
61b
62b
25 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
63b
00 00
00 00
00 00
00 00
00 00
25 00

Fig.7

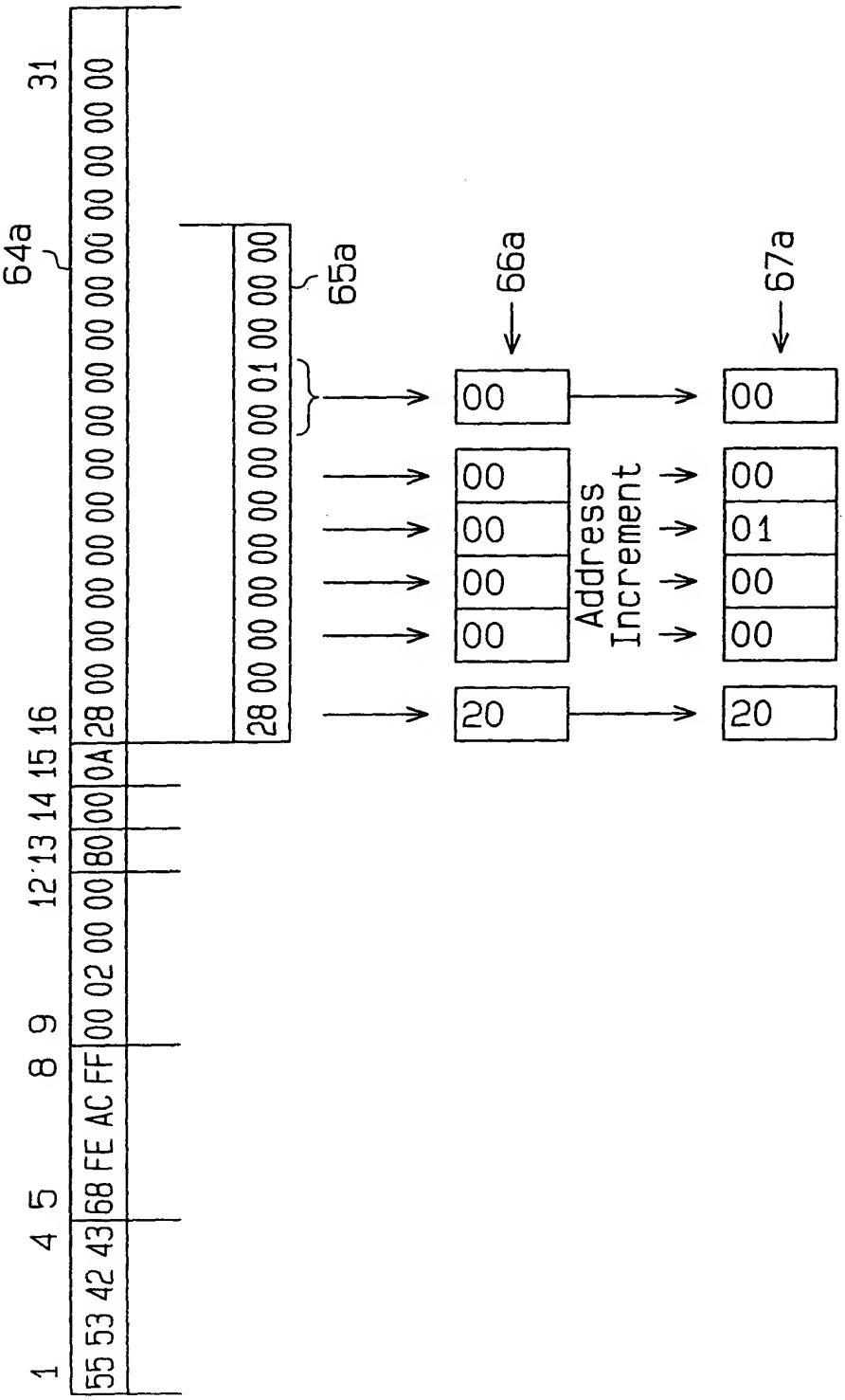
1
4 5
8 9
12 13 14 15 16
31
55 53 42 43 68 FE AC FF 00 02 00 00 80 00 0A 28 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
64a
28 00 00 00 00 00 00 00 00 00 00 01 00 00 00
65a
66a
67a
00
00
00
00
20
Address Increment
00
01
00
00
20

Fig.8

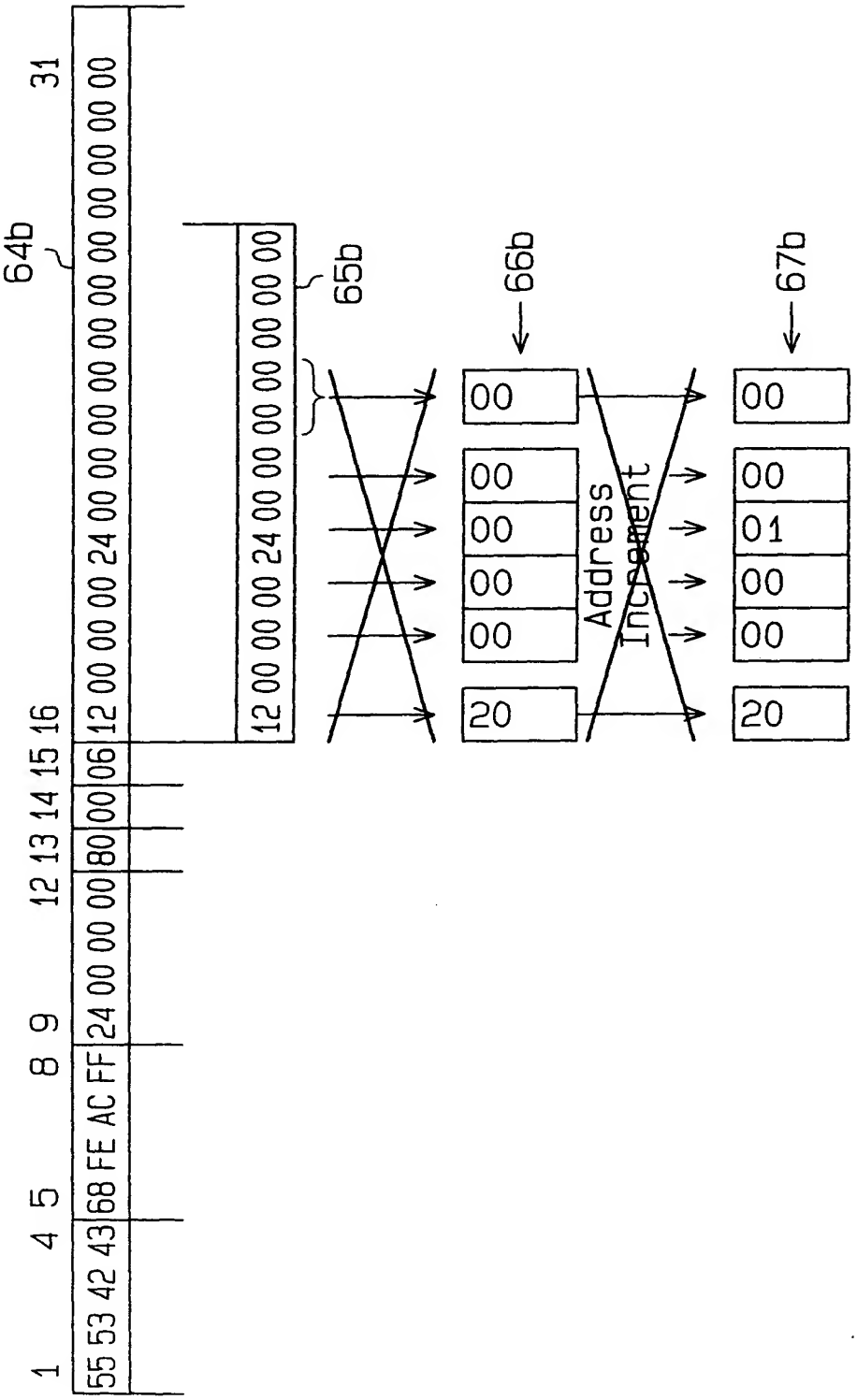
1
4 5
8 9
12 13 14 15 16
31
55 53 42 43 68 FE AC FF 24 00 00 00 80 00 06 12 00 00 00 24 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
64b
65b
66b
67b
12 00 00 00 24 00 00 00 00 00 00 00
00
00
00
00
20
Address Increment
00
00
01
00
00
20

Fig.9

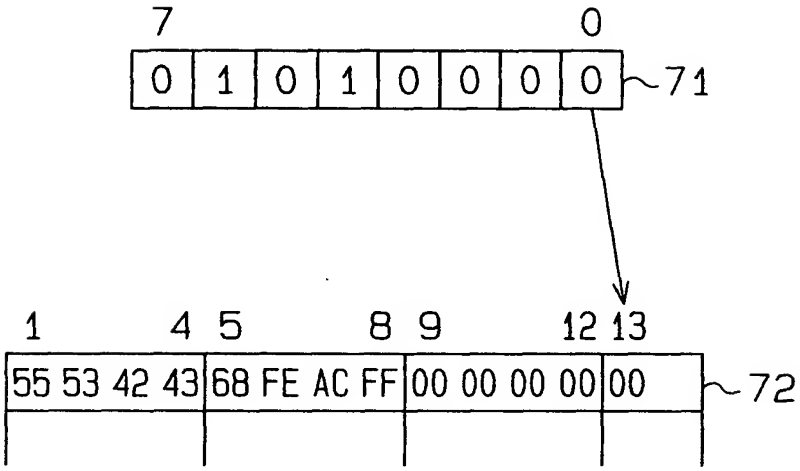
7
0
0 1 0 1 0 0 0 0
71
1
4 5
8 9
12 13
55 53 42 43
68 FE AC FF
00 00 00 00
00
72

Fig.10

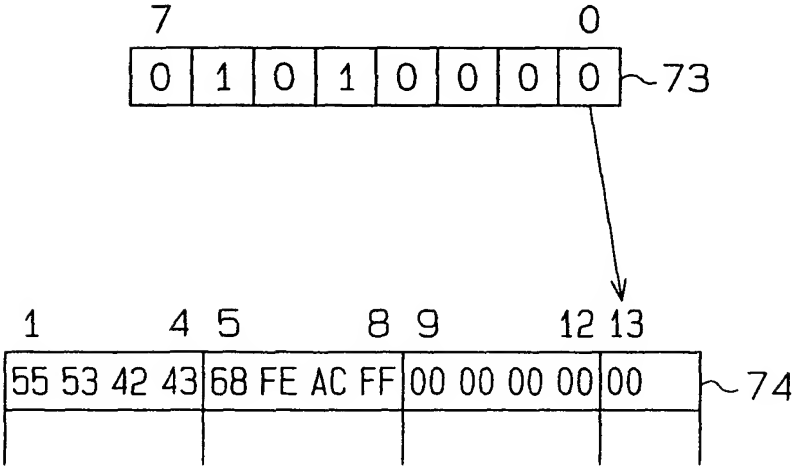
7
0
0 1 0 1 0 0 0 0
73
1
4 5
8 9
12 13
55 53 42 43
68 FE AC FF
00 00 00 00
00
74

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Fig.11

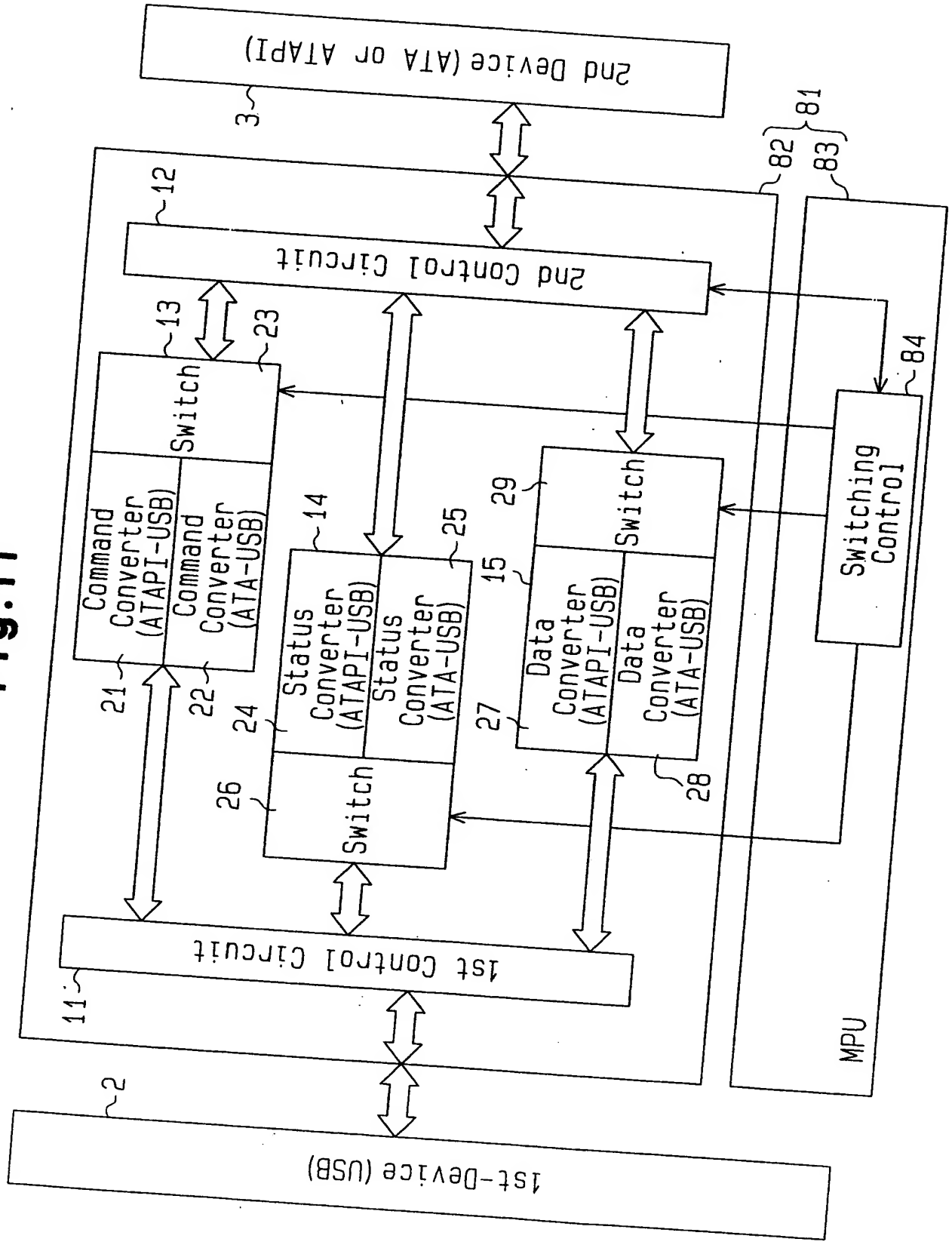

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Fig.12

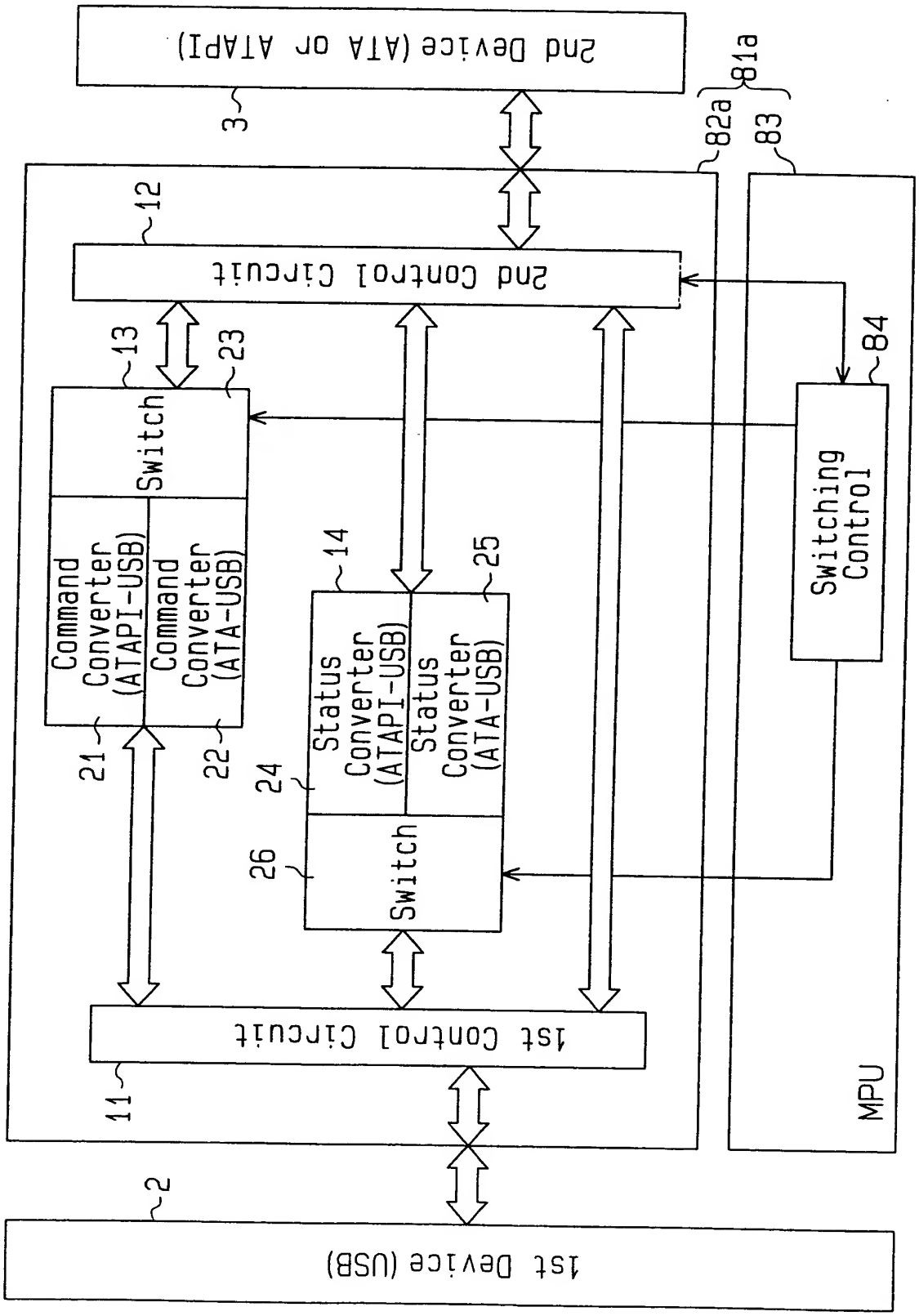

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Fig.13